Application No.: 09/940,324
Amendment dated: November 14, 2005
Reply to Office Action dated: August 11, 2005

REMARKS/ARGUMENTS

Claims 1-17 are pending in the application.

Applicants thank the Examiner for acknowledging acceptance of the Terminal Disclaimer regarding copending application No. 10/231,414.

1. Claim Rejections under 35 U.S.C. §102

Claims 9-15 stand rejected under 35 U.S.C. §102(e) as being unpatentable over U.S. Patent 6,751,705 to Solomon et al.

The Examiner has asserted that Solomon teaches one of a plurality of client ports, referring to Fig. 15, elements 120 and 220 and Fig. 2, element 1600 of Solomon. It appears that the Examiner has tried to read the recited one of a plurality of client ports on a DRAM interface 1600 of the processor bridge 20 of Solomon. The Examiner has also asserted that Solomon teaches a plurality of sub-unit caches, each assigned to one of a plurality of client ports, reading the sub-unit caches on bridge catches 112 shown in Fig. 15 of Solomon. However, Solomon states:

> In one embodiment, (as is shown in FIG. 2), processor bridge logic 20 includes a processor interface 22 designed for the new processor (in one embodiment, the processor bus is called the front-side bus (FSB), and this interface is called the FSB interface (FI)), a bus interface 24 which emulates the bus interface of original processor (in one embodiment, the network bus is called the system-side bus (SB), and this interface is called the SB interface (SI)), a transaction handler 26, and **a DRAM interface (DI) 1600 connected to a bridge cache 112**.

(Solomon, col. 5, lines 22-30, emphasis added).

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> In FIG. 15, memory 16 is distributed across two or more nodes 202.1 to 202.N Each such node 202 includes a memory (116, 216) connected to a node circuit (130, 230). In one bristled node embodiment, each node circuit (130, 230) is connected to two or more processor bridge logics 120, 220. **Each processor bridge logic 220 includes a bridge cache 112** as discussed above. In the embodiment shown in FIG. 15, one processor bridge logic 220 is connected to two processors (118, 119). Each processor includes a Level 0 cache 110 and a Level 1 cache 111. Bridge cache 112 therefore becomes a Level 2 cache. In another embodiment, each processor includes Levels 0-2 cache. Bridge cache 112 therefore becomes a Level 3 cache.

(Solomon, col. 20, lines 55-67, emphasis added).

Accordingly, each processor bridge 20, 120 or 220 in Solomon includes only one bridge cache 112, and only one DRAM interface 1600 connected to the bridge cache 112. Although Solomon may have a plurality of bridge caches 112, each pair of bridge caches 112 and its DRAM interface 1600 belongs to one separate processor bridge. Solomon does not teach any device which has a plurality of DRAM interfaces 1600. Thus, Solomon fails to teach a plurality of sub-unit caches, each assigned to one of a plurality of client ports on an input/output cache-coherent device.

Therefore, Applicants respectfully submit that claims 9-17 are patentable over Solomon.

2. Claim Rejections under 35 U.S.C. §103

A. Claims 1-8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Solomon et al. (Solomon) U.S. Patent No. 6,751,705 in view of Yasuda et al. (Yasuda) U.S. Patent 6,636,926.

The Examiner has tried to read the recited client port on a DRAM interface 1600 of the processor bridge 20 of Solomon, tried to read the recited port components on processors 118 and

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218 shown in Fig. 15 of Solomon, and tried to read the recited sub-unit caches on caches 112 shown in Fig. 15 of Solomon. However, in Solomon, the DRAM interface 1600 is used to couple the cache 112 and the processor bridge 20, instead of coupling the cache 112 and the processors 118 and 218. Solomon fails to teach a plurality of client ports, each to be coupled to one of a plurality of port components.

The Examiner has agreed that Solomon fails to teach a coherency engine coupled to a plurality of sub-unit caches, but has asserted that Yasuda provides this feature, referring to a cache coherence control circuit 330. Applicants respectfully disagree.

Yasuda discloses a shared memory multiprocessor performing cache coherence control. Yasuda describes the cache coherence control circuit 330 with reference to Fig. 4 as follows:

> The cache coherence control circuit 330 is configured with an additional information analysis unit 331 and a cache coherence control request issuing unit 332. The additional information analysis unit 331 checks the contents of the cache coherence control flag included in the additional information held in the access request holding unit 321, and in the case where the cache coherence control flag indicates that the cache coherence control is required, transmits a cache coherence control request from the cache coherence control request issuing unit 332 to the processor.

(Yasuda, col. 11, lines 9-17).

In Yasuda, the cache coherence control circuit 330 works with the access request holding unit 321 to decide whether to transmit a cache coherence control request. Applicants could not find anything in Yasuda supporting the Examiner's argument that the cache coherence control circuit 330 is coupled to a plurality of sub-unit caches.

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Accordingly, Applicants respectfully submit that claims 1-8 are patentable over Solomon and Yasuda.

B. Claims 16-17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Solomon in view of Witt et al (Witt) U.S. Patent 6,202,139.

As discussed above, Solomon fails to teach a plurality of sub-unit caches, each assigned to one of a plurality of client ports on an input/output cache-coherent device as recited in claim 9. Witt fails to supply any deficiencies of Solomon. Witt discloses a pipelined data cache, and states:

> Generally speaking, microprocessor 10 employs a multiported data cache 14, allowing for multiple memory operations to be performed in parallel. The array within data cache 14 is physically single ported, but data cache 14 is pipelined into multiple stages. The pipeline within data cache 14 is operated at a clock frequency which is a multiple of the clock frequency at which the remainder of microprocessor 10 operates.

(Witt, col. 4, lines 42-45).

Accordingly, Witt does not teach a plurality of sub-unit caches, each assigned to one of a plurality of client ports on an input/output cache-coherent device as recited in claim 9 either. Applicants respectfully submit that claims 16 and 17 are patentable over Solomon and Witt.

For all the above reasons, the Applicants respectfully submit that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

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The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to the deposit account of Kenyon & Kenyon, deposit account no. **11-0600**.

Respectfully submitted,

KENYON & KENYON

Dated: November 14, 2005

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